WHAT IS CLAIMED IS:

1. An apparatus for repairing ports of an array to execute instructions, the apparatus comprising:

error logic to determine if a first port of the ports fails;

a swap controller responsive to the error logic to selectively move a first operand to a position of a second operand within the instructions, the position of the second operand being associated with a second port of the ports via the array, to selectively route the first operand and the second operand to the second port depending upon if the first port fails and when execution of at least one of the instructions depends upon transmission of the first operand from the array; and

a selector coupled with the ports, being responsive to the swap controller to selectively receive the first operand from the first port via a first port path and the first operand from the second port via an alternative port path, to execute the instructions.

2. The apparatus of claim 1, further comprising more than one execution units coupled with the selector, wherein the more than one execution units are configured to execute more than one of the instructions in parallel.

3. The apparatus of claim 1, further comprising a swap register coupled with the error logic and the swap controller, to maintain a bit to indicate that the first port failed.

4. The apparatus of claim 3, wherein the bit is set by the error logic to indicate an uncorrectable, hard error associated with the first port.

5. The apparatus of claim 3, wherein the swap register comprises more than one bits to implement more than one mode of operation for the ports.

6. The apparatus of claim 1, wherein the error logic executes an error handler routine to determine if the first port has failed.

7. The apparatus of claim 3, wherein the swap controller routes a first instruction of the instructions in parallel through two pipelines, to route the first operand to the second port.

8. The apparatus of claim 1, wherein the swap controller swaps positions of the first and second operands of two of the instructions, the two instructions to be executed in parallel, to route the first operand to the second port.

9. The apparatus of claim 8, wherein the swap controller swaps the first operand with the second operand before issuing the instructions to an instruction cache.

10. The apparatus of claim 8, wherein the swap controller swaps the first operand with the second operand while the instructions are being issued to an instruction register.

11. An apparatus for repairing ports for a differential memory array, the apparatus comprising:

error logic to determine if a first port of the ports fails;

a swap controller responsive to the error logic to selectively route a first phase bit and a second phase bit consecutively to a second port of the ports, depending upon if the first port fails and when execution of an instruction associated with the first phase bit and the second phase bit depends upon transmission of the first phase bit to a memory cell; and

a selector coupled with the ports, being responsive to the swap controller to selectively receive the first phase bit from the first port via a first port path and the first phase bit from the second port via an alternative port path, to execute the instruction.

12. The apparatus of claim 11, further comprising a differential memory array coupled with the first port and the second port, configured to receive the first phase bit via the first port, the second phase bit from the second port and responsive to the swap controller to receive the both phase bits serially via at least one of the ports.

13. The apparatus of claim 12, wherein the differential memory array is configured to perform a single-ended read based upon the second phase bit from the second port when after the first port fails.

14. A system, comprising:

memory to store instructions;

a register file coupled with the memory to receive the instructions for execution, wherein the register file comprises a first port to transmit a first operand of the instructions and a second port to alternate between transmitting a second operand of the instructions and the first operand, based upon positions of the operands in the instructions;

error logic to determine if the first port failed;

a swap controller coupled with the error logic configured to route the instructions through more than one pipelines for parallel execution, select at least one of the instructions and position operands within the at least one of the instructions, and route the first operand to the second port, in response to a failure of the first port as indicated by the error logic; and

an execution unit coupled with the first port via a first port path and the second port via an alternative port path, wherein the execution unit receives the first operand from the second port via the alternative port path when the first operand is routed to the second port.

15. The system of claim 14, further comprising another execution unit coupled with the second port via the second port path, to receive the second operand.

16. The system of claim 14, wherein the alternative port path facilitates execution of at least two of the instructions in parallel when the first port fails by transmitting the first operand from the second port to the execution unit when execution of at least two instructions depend upon transmission of the first operand and not the second operand.

17. The system of claim 14, wherein the first execution unit couples with the first port and the second port via a port selector, the port selector being responsive to the swap controller to select and forward the first operand to the execution unit via the first port path and the alternative port path.

18. The system of claim 14, wherein the swap controller routes a first instruction of the instructions through at least two pipelines of the more than one pipelines, the first instruction having the first operand.

19. The system of claim 14, wherein the swap controller selectively swaps the positions of the operands in the instructions to alternatively route the first operand and the second operand to the second port and from the second port to the execution unit via the alternative port path and the second port path, in response to a failure of the first port.

20. The system of claim 19, wherein the swap controller selectively swaps the positions of the operands when the instructions are being dispatched to an instruction register.

21. The system of claim 19, wherein the swap controller selectively swaps the positions of the operands as the instructions are stored in an instruction cache.

22. A method for repairing ports of an array, the method comprising:

monitoring transmission from a first port of the ports to detect a failure of the first port;

selectively routing a first operand bound for the first port to a second port of the ports in response to detecting the failure of the first port when execution of an instruction associated with the first operand depends upon receipt of the first operand by a first destination unit;

transmitting the first operand from the second port to the destination unit via an alternative port path; and

transmitting a second operand from the second port to a second destination unit via a second port path.

23. The method of claim 22, wherein monitoring comprises detecting the failure of the first port and initiating a diagnostic routine to determine that the failure is an uncorrectable, hard error.

24. The method of claim 22, wherein selectively routing comprises setting a swap bit, in response to the failure of the first port, and modifying the instruction before the instruction is transmitted to the array, to direct the first operand to the second port via the array.

25. The method of claim 24, wherein modifying the instruction comprises swapping positions of the first operand and the second operand within the instruction.

26. The method of claim 24, wherein modifying the instruction comprises swapping positions of the first operand and the second operand, wherein the first operand is positioned within the instruction and the second operand is positioned within a different instruction to be executed in parallel with the instruction via the array.

27. The method of claim 22, wherein selectively routing comprises routing the first operand and the second operand of the instruction in series to the destination unit via the second port.